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TRANSMITTAL FORM

Attorney Docket No. **29672003RR1737/2345P**

In re the application: **Quiqun Kevin Qi et al.** Confirmation No.: **6766**

Serial No: **10/079,116** Group Art Unit: **2818**

Filed: **February 20, 2002** Examiner: **Pham, Ly D.**

For: **Magnetic RAM Cell with Amplification Circuitry and MRAM Memory Array Formed Using the MRAM Cells**

ENCLOSURES *(check all that apply)*					
☐	Amendment/Reply	☐	Assignment and Recordation Cover Sheet	☐	After Allowance Communication to Group
	☐ After Final	☐	Part B-Issue Fee Transmittal	☐	Appeal Communication to Board of Appeals and Interferences
☐	Information disclosure statement	☐	Letter to Draftsman	■	Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
	☐ Form 1449	☐	Drawings	☐	Status Letter
	☐ (X) Copies of References	☐	Petition	■	Postcard
☐	Extension of Time Request *	☐	Fee Address Indication Form	☐	Other Enclosure(s) (*please identify below):*
☐	Express Abandonment	☐	Terminal Disclaimer		
☐	Certified Copy of Priority Doc	☐	Power of Attorney and Revocation of Prior Powers		
☐	Response to Incomplete Appln	☐	Change of Correspondence Address		
☐	Response to Missing Parts	*Extension of Term: Pursuant to 37 CFR 1.136, Applicant petitions the Commissioner to extend the time for response for xxxxxx month(s), from to .			
	☐ Executed Declaration by Inventor(s)				

CLAIMS					
FOR	Claims Remaining After Amendment	Highest # of Claims Previously Paid For	Extra Claims	RATE	FEE
Total Claims	16	20	0	$18.00	$ 0.00
Independent Claims	3	3	0	$86.00	$ 0.00
				Total Fees	$ 0.00

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☐	Charge $ _____ to Deposit Account No. _____ (Account Holder Name) for payment of fees.
■	Charge any additional fees or credit any overpayment to Deposit Account No. 02-2120 (Sawyer Law Group LLP).

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Attorney Name	Stephen G. Sullivan, Reg. No. 38,329
Signature	
Date	August 18, 2004

CERTIFICATE OF MAILING

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Attorney Docket: 29672003RR1737/2345P

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPEAL NO:

In Re Application of:

Quiqun Kevin QUI, et al.

Serial No.: 10/079,116

Filed: February 20, 2002

Date: August 18, 2004

Confirmation No.: 6766

Group Art Unit: 2818

Examiner: Pham, Ly D.

For: MAGNETIC RAM CELL WITH AMPLIFICATION CIRCUITRY AND MRAM MEMORY ARRAY FORMED USING THE MRAM CELLS

APPELLANT'S BRIEF

Attorney for Appellants
Western Digital Corporation
Sawyer Law Group LLP

TOPICAL INDEX

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Jinny Nguyen

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Application of:	Date: August 18, 2004
Quiqun Kevin QUI, et al.	Confirmation No.: 6766
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APPELLANT'S BRIEF ON APPEAL

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellant herein files an Appeal Brief drafted in accordance with the provisions of 37 C.F.R. § 1.192(c) as follows:

I. REAL PARTY IN INTEREST

Appellant respectfully submits that the above-captioned application is assigned, in its entirety to Western Digital Incorporated of Fremont, California.

II. RELATED APPEALS AND INTERFERENCES

Appellant states that, upon information and belief, he is not aware of any co-pending appeal or interference which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1, 2, 3, 4, 5, 6, 7, 8, and 9 are pending. Application Serial No. 10/079,116 (the instant application) as originally filed included claims 1-21. In a response to a Restriction Requirement, Appellant elected claims 1-9, with traverse. In response to an Office Action dated September 12, 2003, the allowability of claims 1-9 was argued, but claims 1-9 were not amended. Similarly, in response to the Final Office Action dated January 22, 2004, the allowability of claims 1-9 was again argued, but claims 1-9 were not amended. Claims 1, 2, 3, 4, 5, 6, 7, 8, and 9 are on appeal and all applied prospective rejections concerning claims 1-9 are herein being appealed.

IV. STATUS OF AMENDMENT

There was no proposed Amendment to claims 1-9 in response to the Final Office Action dated January 22, 2004.

V. SUMMARY OF THE INVENTION

The present invention provides an improved magnetic memory cell and a magnetic memory using the magnetic memory cell. In one aspect, the magnetic memory cell includes a magnetic tunneling junction (MTJ) and a transistor. The MTJ includes first and second

ferromagnetic layers and an insulating layer therebetween. The transistor includes a source, a drain, and a gate. The gate of the transistor is coupled to a first end of the MTJ, while the source of the transistor is coupled to a second end the MTJ. The drain of the transistor is coupled with an output for reading the magnetic memory cell.

In another aspect, the present invention provides a magnetic memory. The magnetic memory includes a plurality of memory cells arranged in an array having rows and columns. Each of the memory cells includes a MTJ and a transistor. The magnetic tunneling junction and transistor are as described above. The magnetic memory also includes a plurality of row lines coupled to the gate of the transistor in each of the memory cells in the rows. A row selector is coupled to the plurality of row lines for selecting between the plurality of row lines and providing a current to a selected row of the plurality of rows.

One embodiment of a magnetic memory cell in accordance with the present invention is depicted in Figure 1 of the present application. Figure 1 includes a memory cell 100 having a MTJ 104 and a transistor 102. A memory incorporating the memory cell 100 is depicted in Figure 4. Figures 5A and 5B are drawings depicting physical locations of the layers in the MTJ 104 and the transistors 102. Because of the connections between the transistor, the portions of the MTJ, and the output, the magnitude of the signal is increased. Furthermore, the difference in signal between the small resistance and high resistance states is significantly larger. Specification, page 7, lines 16-24. In addition, reliability is improved. Specification, page 10, lines 20-21.

VI. ISSUES

The issues presented are:

(1) whether claims 1, 2, 3, 4, 5, 6, 7, 8, and 9 are each unpatentable under 35 U.S.C. § 103 over JP 411204854A (Mizushima).

VII. GROUPING OF CLAIMS

Claims 1, 2, 3, 4, 5, 6, 7, 8, and 9 constitute one (1) group for the purposes of this appeal.

VIII. ARGUMENTS

A. Summary of the Applied Rejections

In the Final Office Action, dated January 22, 2004 the Examiner rejected claims 1-9. The Examiner rejected claims 1-9 under 35 U.S.C. § 103 as being unpatentable over Mizushima. The Examiner cited Figure 10 of Mizushima, item 4 as teaching the recited MTJ and item 2 as teaching the recited resistor, including the recited connections between the magnetic tunneling junction and the resistor.

In response to Appellant's previous arguments, the Examiner stated:

> **With respect to item 4 being termed as [sic] "gate resistor", the Office would like to point out that 4 was labeled for the gate resistor of fig. 1. In Mizushima's circuit configuration of fig. 1, the gate resistor 4 together with the MTJ 1 are used to divide the word line voltage feeding to the gate of the memory transistor, for the identical purpose as recognized by the claimed feature, in which wider margin of the signal between the different states of the output as a result would improve performance. Here, the drawing for the MTJ is similarly [sic] to a variable resistor. In fig. 10, Mizushima shows another variation of the same inventive concept in which the "gate resistor" is replaced by transistor 9 for even more stabilized operation from the identical concept and the MTJ is nevertheless labeled 4 (here, 4 is drawn identically to 1 in fig. 1).**
>
> **From another view point, it is inherent in magnetic memory specifications that in fig. 10, 4 has to be a MTJ because if 4 was not, there is no other place in the drawing of the memory cell of fig 10 [that] would an MTJ be [sic] and that simply does not make sense for magnetic memory cell [to be] without an MTJ, or TMR (tunneling magneto resistor), which is essential for storing data.**

With respect to claims 4 and 9, the Examiner took Official Notice that the claimed limitation, the transistor operating in the saturation regime, is well known in the art.

Appellant respectfully requests that the Board reverse the Examiner's final rejection of claims 1, 2, 3, 4, 5, 6, 7, 8, and 9 under 35 U.S.C. § 103.

B. The Cited Prior Art

The Abstract of Mizushima clearly states that the components of one memory cell of Mizushima includes a transistor 2, an MTJ 1 connected to the gate of the transistor 2, and a "gate resistor" 4. This configuration can clearly be seen in Fig. 1 of Mizushima, which depicts the MTJ 1 connected to the gate of the transistor 2. Also included is the gate resistor 4. Appellant notes that, as one of ordinary skill in the art would readily understand, an MTJ functions by having a resistance that varies with the magnetic state of the MTJ. Consequently, an MTJ is one type of variable resistor. As a result, in the circuit diagram shown in Fig. 1 of Mizushima, the well known symbol for a variable resistor is used for the MTJ 1.

In the computer translation of Mizushima, it is also stated that drawing 1 includes the MTJ 1(termed a magnetic-substance tunnel junction in the computer aided translation of Mizushima), the gate resistance 4, and the transistor 2. See Paragraphs 46-47 of Mizushima, computer aided translation.

Fig. 10 of Mizushima, cited by the Examiner, is also described in the computer aided translation of Mizushima. In particular, it is stated that:

> The magnetic memory cell which starts the 2nd operation gestalt of this invention at drawing 10, is shown. In addition, **the same sign as drawing 1** is given to the magnetic memory cell of drawing 1, and the corresponding portion, and detailed explanation **is omitted**.
>
> This operation gestalt is the example in which used the **hot electron transistor as a GMR element**. A hot electron transistor is a GMR element which shows bigger MR ratio than a magnetic-substance tunnel junction element MR. MR ratio of a hot electron transistor exceeds 200%. Therefore, it becomes easier to read the information on a memory cell correctly, and it can lessen a read error. . .

> For this reason, like the case of a magnetic-substance tunnel junction element, in order to carry out high-speed operation about ns, as shown in drawing 10 </A>, connecting with the gat of MOS transistor 2 is desirable [a hot electron transistor 9 (collector)].

Paragraphs 82-85, Mizushima, computer aided translation (boldface added). Thus, Fig. 10 of Mizushima depicts a hot electron transistor 9 functioning as a memory element in a memory cell. The remaining portions of the cell in Fig. 10 of Mizushima correspond to portions of Fig. 1 of Mizushima and are thus not described in great detail. Consequently, Fig. 10 of Mizushima also includes a transistor 2 and a gate resistance 4 that happens to be a variable gate resistance as indicated by the arrow through the resistor symbol.

C. Claims 1-9 Are Not Unpatentable Under 35 U.S.C. § 103.

Appellant respectfully submits that the Examiner's rejections of claims 1-9 under 35 U.S.C. § 103 are improper because they are based on and require an erroneous assumption about what Mizushima teaches. In fact, Mizushima neither teaches nor suggests a memory cell including an MTJ and a transistor in which:

> the gate of the transistor being coupled to a first end of the magnetic tunneling junction, the source of the transistor being coupled to a second end the magnetic tunneling junction, the drain of the transistor being coupled with an output for reading the magnetic memory cell

as independent claims 1 and 5 require.

As discussed above, Fig. 1 of Mizushima discloses a cell which includes the MTJ 1, a transistor 2 and a gate resistor 4. Abstract, Mizushima. As can be seen in Fig. 1, the cell of Mizushima does not have the gate and source of the transistor 2 coupled with opposing ends of the magnetic tunneling junction 1 in combination with the drain of the transistor 2 connected to the output. Instead, one end of the MTJ 1 is connected to the gate of the transistor 2, while the other

end of the MTJ 1 is connected to the word line WL. The source of the transistor 2 is connected to the output V_o, while the drain is connected to ground. Thus, Fig. 1 of Mizushima fails to teach or suggest the memory cell recited in claim 1 and the memory recited in claim 5.

Fig. 10 of Mizushima also fails to teach or suggest the recited memory cell and transistor. As is clearly indicated in the computer aided translation of Mizushima, the memory element in Fig. 10 of Mizushima is the hot electron transistor 9. As is also clear from the computer aided translation of Mizushima, the remaining components correspond to the components in Fig. 1 having similar numerical designations. Consequently, item 4 of Fig. 10 is a (variable) gate resistor, while item 2 is a transistor. Furthermore, even without the computer aided translation of Mizushima, there is no reason to believe that Mizushima would use a particular number to designate one type of component in Fig. 1, then use exactly the same number to designate a different type of component in Fig. 10. Consequently, item 4 of Fig. 10 of Mizushima is still a (variable) gate resistor. Fig. 10 of Mizushima thus does not include an MTJ. Consequently, Fig. 10 of Mizushima fails to teach or suggest the recited combination of the MTJ and transistor and connections therebetween of independent claims 1 and 5.

The fact that the same symbol, a resistor with an arrow through it, is used to designate the MTJ 1 of Fig. 1 and the gate resistor 4 of Fig. 10 does not alter this conclusion. Appellant respectfully submits that one of ordinary skill in the art would readily recognize that such a symbol is routinely used for any variable resistor. The symbol is used for the MTJ 1 in Fig. 1 of Mizushima because the resistance of the MTJ varies. However, numerous variable resistors which are not MTJs also exist. Consequently, another variable resistor can be represented by the same symbol as is used for the MTJ 1. This occurs in Fig. 10 of Mizushima in which the gate resistance is represented by the same symbol. This also occurs in Fig. 13, which also uses a variable gate

resistance 4. Moreover, Appellant notes that Fig. 12 includes an MTJ that is, therefore, designated with the numeral "1". Appellant respectfully submits that it is the item designation number (1), not the symbol design (resistor symbol with an arrow through it), that indicates what the item is. Consequently, the use of the same symbol for the gate resistor 4 and the MTJ 1 does not alter the conclusion that Fig. 10 does not include an MTJ. Fig. 10 of Mizushima still fails to teach or suggest the recited combination of the MTJ and transistor in independent claims 1 and 5. Claims 1 and 5 are thus allowable over the cited references. Accordingly, Appellant respectfully requests that the Board reverse the final rejection of claims 1 and 5.

Claims 2, 3, and 4 depend on independent claim 1. Claims 6, 7, 8, and 9 depend upon independent claim 5. Consequently, claims 2-4 and 6-9 are allowable for the same reasons discussed above with respect to claims 1 and 5, respectively.

Accordingly Appellant respectfully requests that the Board reverse the final rejection of claims 1, 2, 3, 4, 5, 6, 7, 8, and 9 under 35 U.S.C. § 103.

E. Summary of Arguments

For all the foregoing reasons, it is respectfully submitted that Claims 1, 2, 3, 4, 5, 6, 7, 8, and 9 (all the claims presently in the application) are patentable for defining subject matter which would not have been obvious under 35 U.S.C. § 103. Thus, Appellant respectfully requests that the Board reverse the rejection of all the appealed Claims and find each of these Claims allowable.

Note: For convenience of detachment without disturbing the integrity of the remainder of pages of this Appeal Brief, Appellant's "APPENDIX" section is contained on separate sheets following the signatory portion of this Appeal Brief.

This Brief is being submitted in triplicate, and authorization for payment of the required Brief fee is contained in the cover letter for this Brief. Please charge any fee that may be necessary for the continued pendency of this application to Deposit Account No. 02-2120 (Sawyer Law Group LLP).

Respectfully submitted,
SAWYER LAW GROUP LLP

August 18, 2004
Date

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IX. APPENDIX

1. A magnetic memory cell comprising:

a magnetic tunneling junction including a first ferromagnetic layer, a second ferromagnetic layer and an insulating layer between the first ferromagnetic layer and the second ferromagnetic layer; and

a transistor having a source, a drain and a gate, the gate of the transistor being coupled to a first end of the magnetic tunneling junction, the source of the transistor being coupled to a second end the magnetic tunneling junction, the drain of the transistor being coupled with an output for reading the magnetic memory cell.

2. The magnetic memory cell of claim 1 wherein the transistor is a MOSFET or another type of transistor.

3. The magnetic memory cell of claim 1 wherein a second end of the magnetic tunneling junction and the source of the transistor are coupled to ground.

4. The magnetic memory cell of claim 1 wherein the transistor is operated in a saturation region during reading.

5. A magnetic memory comprising:

a plurality of memory cells arranged in an array including a plurality of rows and a plurality of columns, each of the plurality of memory cells including a magnetic tunneling

junction and a transistor having a source, a drain and a gate, the gate of the transistor being coupled to a first end of the magnetic tunneling junction, the source of the transistor being coupled to a second end of the magnetic tunneling junction, the drain of the transistor being coupled with an output for reading the magnetic memory cell;

a plurality of row lines coupled to the plurality of rows, the plurality of row lines coupled to gate of the transistor in each of the plurality of memory cells in the plurality of rows;

a row selector coupled to the plurality of row lines for selecting between the plurality of row lines and providing a current to a selected row of the plurality of rows.

6. The magnetic memory of claim 5 further comprising:

a first plurality of column lines coupled to the plurality of columns, the plurality of columns lines coupled to source of the transistor in each of the plurality of memory cells in the plurality of columns;

a second plurality of column lines coupled to the plurality of columns, the second plurality of column lines coupled to the drain of the transistor in each of the plurality of memory cells in the plurality of columns, each of the first plurality of columns lines coupled to a particular column, a corresponding column line of the second plurality of column lines coupled to the particular column line, each of the first plurality of column lines and the corresponding column line of the second plurality of column lines forming a pair of column lines;

a column selector coupled to the first plurality of column lines and the second plurality of column lines for selecting between the first plurality of column lines and the second plurality of column lines to select a pair of column lines.

7. The magnetic memory of claim 5 further comprising:

a plurality of digit lines for providing a current for writing to a portion of the plurality of memory cells.

8. The magnetic memory of claim 6 further comprising a load coupled to the plurality of column lines.

9. The magnetic memory of claim 5 wherein the transistor is operated in a saturation region during reading.